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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,645	02/24/2004	Hartmut B. Brinkhus	VBW 5635	2374

321 7590 09/20/2006

SENNIGER POWERS
ONE METROPOLITAN SQUARE
16TH FLOOR
ST LOUIS, MO 63102

EXAMINER	
VIDWAN, JASJIT S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,645	BRINKHUS, HARTMUT B.	
	Examiner	Art Unit	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/24/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/18/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because they lack labels with functional description. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. Since claims 2-19 depend from Claim 1, Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: plurality of multiplexers, analog comparator and digital/analog converter are all individually claimed elements that are not connected with the overall claimed system. Applicant claims that the multiplexers **can be** controlled

by **signals**. It is unclear to the examiner whether the Applicant intents to tie in the said multiplexers with previously mentioned signals that control the switches, which therein are connected to bidirectional input connection (i.e. plurality of multiplexers are "connected directly or indirectly to at least one input connection"). Furthermore, the analog comparator and digital/analog converter both lack relationship to any other elements of the system.

4. Claim 1 recites the limitation "**the components**" in line 15 of Claim 1. There is insufficient antecedent basis for this limitation in the claim. It is unclear to the Examiner which components the Applicant is referring to, however for the purpose of timely examination of the Application, the Examiner will construe the components to refer to the switches, multiplexers or either input or output connections.

5. Regarding claims 3 and 4, the phrase **"i.e."** renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Schloterer et al U.S. Patent No: 5,751,234 [herein after Schloterer].

8. **As per Claim 1**, Schloterer teaches an interface circuit **[Col. 1, Lines 20-29, "Integrated Circuit"]** for process connections to computer, the interface circuit comprising:

> (a) At least one input connection **[Fig. 2, element 52, "Port A" – Also see Col. 23, Lines 4-5]**
>
> (b) At least one output connection **[Fig. 2, element 54, "Port B" – Also see Col 23, Lines 53-55]**, which is connected to a logic circuit **[Fig. 2, Element 30, "Microprocessor"]**.

(c) Plurality of switches **[Fig. 3, Elements 108, 110, 112]**, which can be controlled by signals, whose inputs are connected directly or indirectly to at least one input connection **[see Fig. 2, *elements 62 and 64 whose representation is shown in detail in Fig 3 is connected to I/O Ports A, B and C via "Data & Control Bus"*]**.

(d) Several multiplexers, which can be controlled by signals **[Fig. 3, Elements 102, 104, 106]**.

(e) At least one analog comparator **[Fig. 2, elements 50 and 58]**

(f) At least one digital/analog converter **[Col. 56, Lines 40-42]**

(g) Wherein according to the state of one or more of the signals which control the switches and multiplexers **[Col. 38, Lines 29-30, *"Signal SAMPh which controls the sample and hold switches 108, 110 and 112"*]** the switches are activated, deactivated, or changeable into different operating or switching states, with different analog or digital functions being assignable to the one or more bidirectional input connection **[Col. 34, Lines 35-39]**

9. **As per Claim 2**, Schloterer teaches an interface circuit wherein the one or more bidirectional output connections are connected over a decoupling device to the logic circuit **[Col. 23, Lines 58-62]**.

10. **As per Claim 3 and 4**, Schloterer teaches an interface circuit wherein the multiplexers can be operated bidirectionally **[Col. 7, Lines 42-46]**

11. **As per Claim 5**, Schloterer teaches an interface circuit wherein the one or more analog comparators are associated with a sample-and-hold circuit, whose input is connected to at least one input connection **[Col. 38, Lines 26-28]**.

12. **As per Claim 6**, Schloterer teaches an interface circuit wherein the one or more analog/digital converters operate according to the principle of successive approximation **[Col. 56, Lines 40-42, *'The A/D converter is an eight bit successive approximation A/D converter.'*]**

13. **As per Claim 7**, Schloterer teaches an interface circuit wherein between the one or more input connections are one or more analog comparators, a current/voltage converter is connected with the connection being switchable by the multiplexer **[Col. 1, Lines 41-48]**.

14. **As per Claim 8**, Schloterer teaches an interface circuit wherein one or more of the analog comparators are connected after the controllable hysteresis circuit **[see Fig. 2, elements 50 and 58]**.

15. **As per Claim 9**, Schloterer teaches an interface circuit wherein a digital/analog converter is connected in the signal direction from the output connection to one or more input connections, with the connection being switchable in a controlled way by the multiplexer **[Col. 7, Lines 34-46]**.

16. **As per Claim 10**, Schloterer teaches an interface circuit, wherein at least two input connections are connected to each other over a measurement resistor and a controllable switch, with both connections of the measurement resistor being connected to a differential amplifier, whose output is connected to one or more analog/digital converters **[See Fig. 3, elements 84 and 80].**

17. **As per Claim 11, 12 and 13**, Schloterer teaches an interface wherein several interface circuits are connected in a cascade arrangement and connected to the logic circuit **[see Fig. 1, element 12]**

18. **As per Claim 14 and 15**, Schloterer teaches an interface wherein a decoupling device is connected between the interface circuit and the logic circuit **[Fig. 3, element 90]**

19. **As per Claim 16**, Schloterer teaches an interface circuit wherein higher functions are implemented in the logic circuit **[Col, 13, Lines 55-59]**, while only functions are implemented in the interface circuit **[Col. 1, Lines 21-29]**.

20. **As per Claim 17**, Schloterer teaches an interface circuit wherein the higher functions comprise system functions **[Col, 13, Lines 55-59]**.

21. **As per Claim 18 and 19**, Schloterer teaches an interface circuit wherein the logic circuit and the interface circuit are configured such that bidirectional serial communication takes place between these circuits **[Col. 10, Lines 18-23]**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
9/12/06

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